What is claimed is:

1. A header of a nano storing apparatus comprising:

a cantilevery array including cantilevers each having a probe that is able to read and write information with the 'n' number of rows and the 'm' number of columns (n, m = 1, 2, 3, ...);

an X-redundancy cantilever array to be used as a substitute when cantilever probes of a specific row in the cantilever array are defective;

a Y-redundancy cantilever array to be used as a substitute when cantilever probes of a specific column in the cantilever array are defective; and

a header controller for controlling each part.

2. The header of claim 1, wherein the header controller comprises:

the X-decoder for receiving an X-address signal and driving cantilevers of a specific row in the cantilever array;

the X-redundancy decoder for stopping driving of the X-decoder when cantilevers of a specific row in the cantilever array are defective and selecting the X-redundancy cantilever array;

the Y-decoder for receiving an Y-address signal and selectively driving a specific column in the cantilever array; and

the Y-redundancy decoder for stopping driving of the Y-decoder when cantilevers of a specific column in the cantilever array are defective, and selecting the Y-redundancy cantilever array.

3. The header of claim 2, wherein the X-redundancy decoder stops

driving of the X-decoder when the X-redundancy cantilever array is selected.

4. The header of claim 2, wherein the X-redundancy decoder comprises:

an output terminal for outputting a stop signal to the X-decoder when cantilevers of a specific row in the cantilever array are defective;

a unit for transferring a high voltage (V_{CC}) to the output terminal by a specific pulse signal (XRP);

a unit for receiving the X-address signal and outputting a low voltage (0V) to the output terminal; and

a plurality of fuses connected between the output terminal and the unit which outputs the low voltage, and selectively defused when cantilevers of a specific row in the cantilever array are defective.

5. The header of claim 4, wherein the X-redundancy decoder converts signal values received from the high voltage outputting unit and the low voltage outputting unit into logical values and outputs the corresponding signal values to the X-decoder and the X-redundancy cantilever array.

6. The header of claim 4, wherein as the fuse, a polysilicon line or a metal line is used, and the fuse can be melt by using an overcurrent, cut by laser beam or programmed by an EPROM memory cell.

7. The header of claim 2, the header controller further comprises:

a Y-switch for receiving an output signal of the Y-decoder when

cantilevers of a specific column in the cantilever array are defective, and cutting off a data output of the defective cantilevers of the specific column; and

a Y-redundancy switch for receiving an output signal of the Y-redundancy decoder when cantilevers of a specific column in the cantilever array are defective, and switching a data output of the Y-redundancy cantilever array.

8. The header of claim 7, wherein when the Y-redundancy cantilever array is selected, the Y-redundancy decoder stops driving of the Y-decoder and outputs a signal for selecting the Y-redundancy switch.

9. The header of claim 2, wherein the Y-redundancy decoder comprises:

an output terminal for outputting a stop signal to the Y-decoder when cantilevers in a specific column in the cantilever array are defective;

a unit for outputting a high voltage (V_{CC}) to the output terminal by a specific pulse signal (YRP);

a unit for receiving a Y-address signal and outputting a low voltage (0V); and

a plurality of fuses connected between the output terminal and the low voltage outputting unit, and selectively defused when cantilevers of a specific column in the cantilever array are defective.

10. The header of claim 1, wherein the X-redundancy cantilever array includes the 'p' number of rows and the 'm' number of columns ($p \leq n$, p=1, 2, 3..), and if cantilever probes of a specific row in the cantilever array having the nxm

number of cantilevers are defective, cantilevers of a specific row of the X-redundancy cantilever array are substitutively used, and meanwhile, the Y-redundancy cantilever array includes the 'n' number of rows and the 'k' number of columns ($k \leq m$, k=1, 2, 3, ...), and if cantilever probes of a specific column in the cantilever array having the nxm number of cantilevers are defective, cantilevers of a specific column in the Y-redundancy cantilever array are substitutively used.

11. A header of a nano storing apparatus comprising:

a cantilever array having cantilevers of the 'n' number of rows and cantilevers of the 'm' number of columns;

an X-redundancy cantilever array having cantilevers to be substitutively used when cantilevers of a specific row in the cantilever array are defective;

a Y-redundancy cantilever array having cantilevers to be substitutively used when cantilevers of a specific column in the cantilever array are defective;

an X-decoder for receiving an X-address signal and driving cantilevers of a specific row in the cantilever array;

an X-redundancy decoder for stopping driving of the X-decoder when cantilevers of a specific row in the cantilever array are defective, and selecting the X-redundancy cantilever array;

a Y-decoder for receiving a Y-address signal and driving cantilevers of a specific column in the cantilever array; and

a Y-redundancy decoder for stopping driving of the Y-decoder when cantilevers of a specific column in the cantilever array are defective, and selecting the Y-redundancy cantilever array.

12. The header of claim 11, wherein the X-decoder includes NAND gates and inverters connected to the NAND gates, and drives the cantilever array upon receiving the X-address signal or stops the cantilever array upon receiving a signal from the X-redundancy decoder.

13. The header of claim 11, wherein the X-redundancy decoder comprises:

an output terminal for outputting a stop signal to the X-decoder when cantilevers of a specific row in the cantilever array are defective;

a unit for transferring a high voltage (Vcc) to the output terminal by a specific pulse signal (XRP);

a unit for receiving the X-address signal and transferring a low voltage (0V) to the output terminal; and

a plurality of fuses connected between the output terminal and the low voltage transferring unit and selectively defused when cantilevers of a specific row in the cantilever array are defective.

14. The header of claim 11 further comprising:

a Y-switch for receiving an output signal of the Y-decoder when cantilevers of a specific column in the cantilever array are defective, and cutting off a data output of the defective cantilevers of the specific column; and

a Y-redundancy switch for receiving an output signal of the Y-redundancy decoder when cantilevers of a specific column in the cantilever array are defective, and switching a data output of the Y-redundancy cantilever array.

15. The header of claim 14, wherein the Y-decoder is provided as many as columns in the cantilever array in order to drive cantilevers of each column, and the Y-redundancy decoder is connected to each Y-decoder and provided as many as columns in the cantilever array in order to enable a data output to or stop data output from cantilevers of a specific column in the cantilever array.

16. The header of claim 15, wherein the Y-decoder comprises:

NAND gates for receiving the Y-address signal and a signal from the Y-redundancy decoder and turning on or off a switch of the Y-switch in order to enable a data output to or stop data output from cantilevers of a specific column in the cantilever array; and

Inverters connected to the NAND gates.

17. The header of claim 15, wherein the Y-redundancy decoder comprises:

a unit for transferring a high voltage (Vcc0 to the output terminal by a specific pulse signal (YRP);

a unit for receiving the Y-address signal and transferring a low voltage (0V) to the output terminal through a fuse; and

an inverter for inverting an output of the output terminal and outputting it to the Y-decoder.

18. The header of claim 17, wherein the fuse is connected between the output terminal and the low voltage outputting unit, and selectively defused

when cantilevers of a specific column in the cantilever array are defective.